MATSUDA
GRAYSON

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(54) Apparatus for controlling production of speech or text

(57) To enable a physically severely disabled person to produce messages in the form of speech or printed text, a central processor 29 is provided with a program in a read only memory 34 which includes look-up tables of ASCII codes for a speech synthesizer unit or a printer. The appropriate look-up table is addressed by computing the required address from the coordinates of a selected display element of a LED matrix indicator 19, the selected element displaying a message element chosen by the user by operation of two input switches of input circuitry 45. The program also enables series of coordinates of successive LEDs selected in the matrix indicator 19 to be stored in temporary RAM stores and recalled subsequently as required, with retrieval of corresponding ASCII codes during the recall so that a stored message can be replayed as speech or printed text when required.

spec p2, lines 13-22

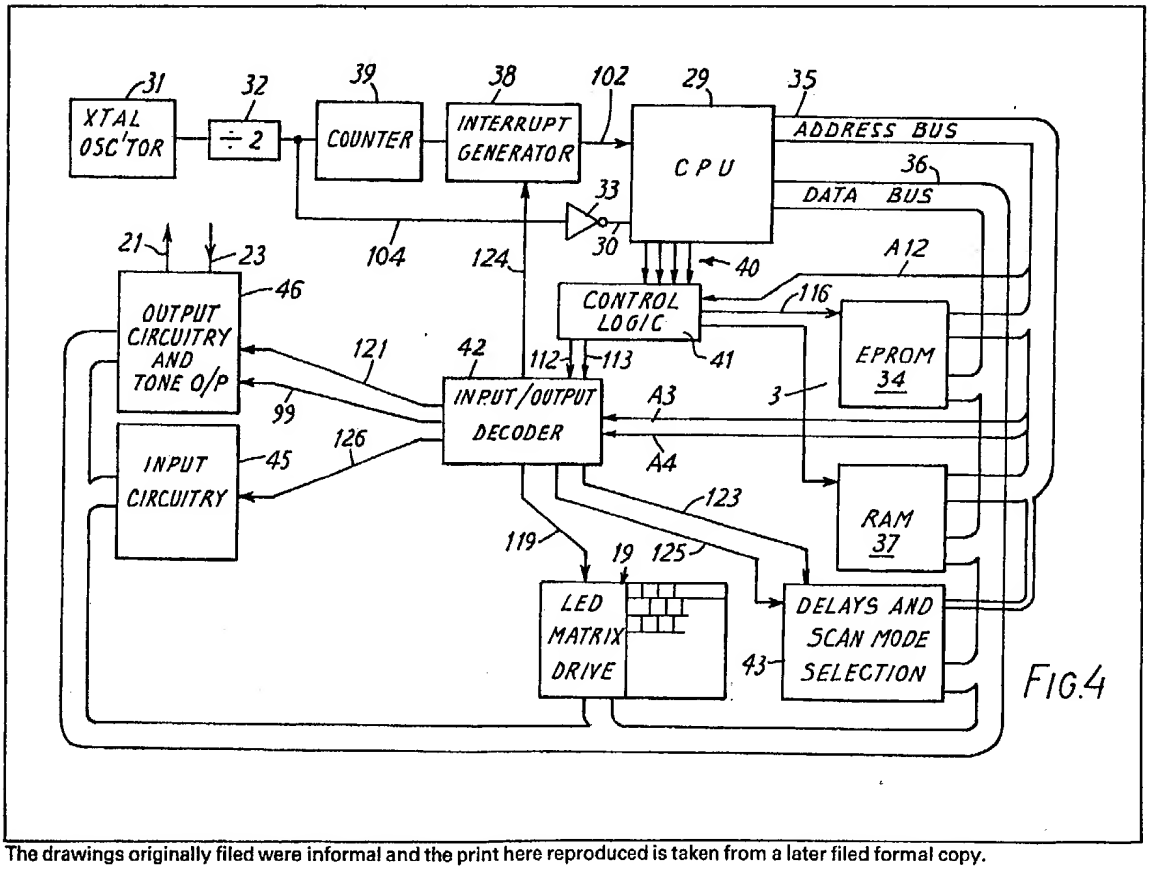

FIG.4

GB 2 128 786 A

The drawings originally filed were informal and the print here reproduced is taken from a later filed formal copy.

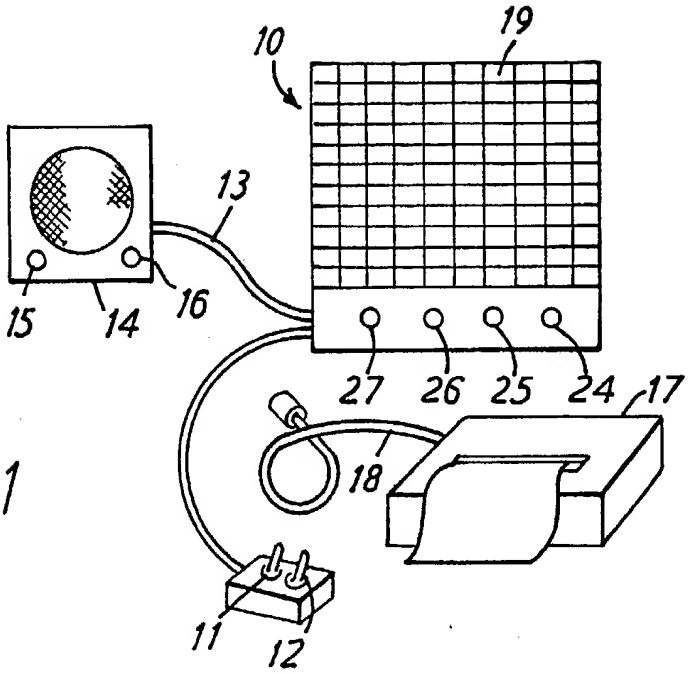
10
19
13
15
14
16
27
26
25
24
17
18
11
12

FIG. 1

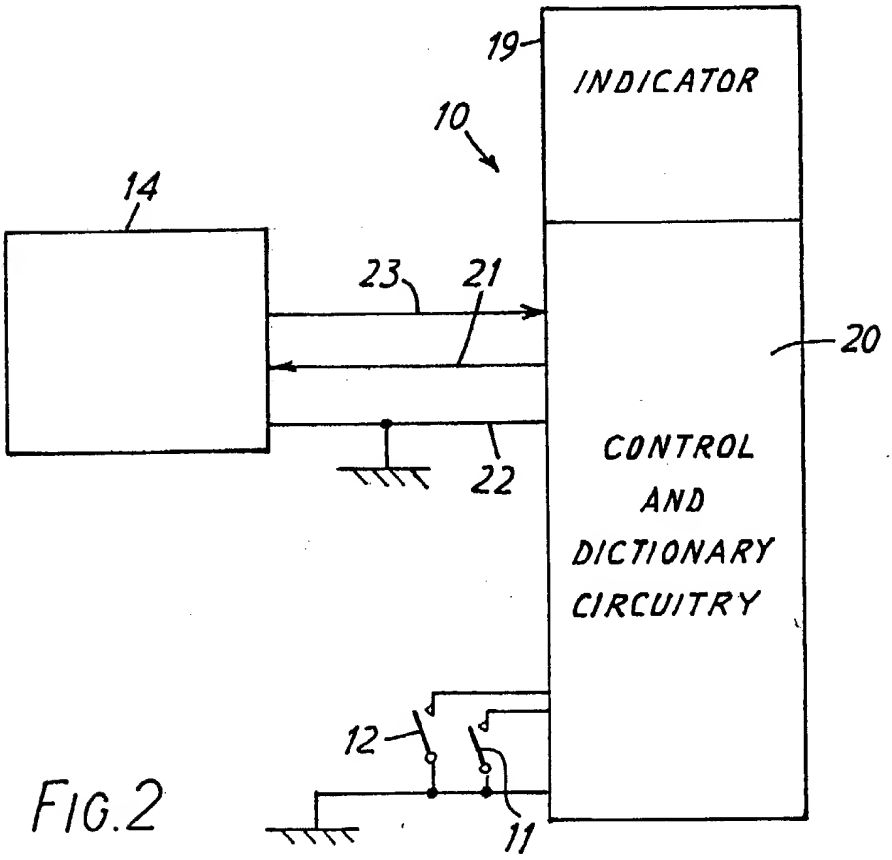
19
INDICATOR
10
14
23
21
20
CONTROL
AND
DICTIONARY
CIRCUITRY
22
12
11

FIG. 2

HOME SQUARE	SHIFT	SPACE	CARRIAGE RETURN	DELETE	SELECT OVERLAY	TONE ON/OFF	FEED		
A	a afternoon of yes	b	c						
B	j brown plain	k	1						
C	s chocolate sandals	t	u	v	w	x	y	z	ϕ
D	1 dress sick	2	3	4	5	6	7	8	9
MEMORY READ	, go stockings sunday	.	?						
MEMORY WRITE	red hello the C.S.R.	orange	yellow						
SPEAK	in to R.A.								
PRINT	lemon turkey								
CALL	medicine was								

C.S.R. = Change Scan Rate R.A. = Read Aloud

FIG.3

2/10

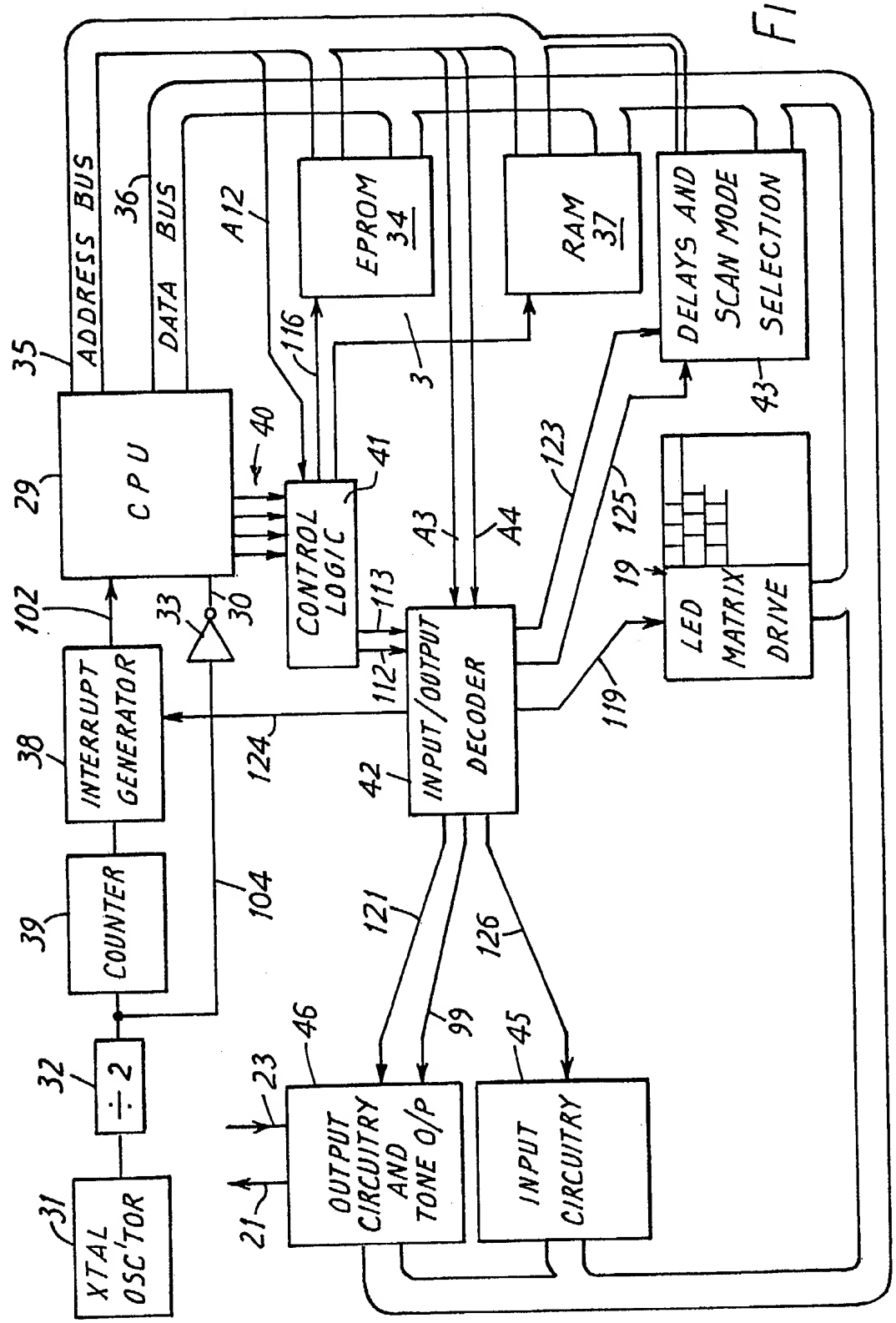
ADDRESS BUS
35
DATA BUS
36
A12
EPROM 34
RAM 37
DELAYS AND SCAN MODE SELECTION
43
116
3
C P U
29
40
41
CONTROL LOGIC
A3
A4
123
125
19
LED MATRIX DRIVE
102
33
30
113
INPUT/OUTPUT DECODER
112
119
INTERRUPT GENERATOR
38
124
42
COUNTER
39
104
121
126
32
÷ 2
46
99
45
23
OUTPUT CIRCUITRY AND TONE O/P
INPUT CIRCUITRY
21
31
XTAL OSC'TOR

FIG.4

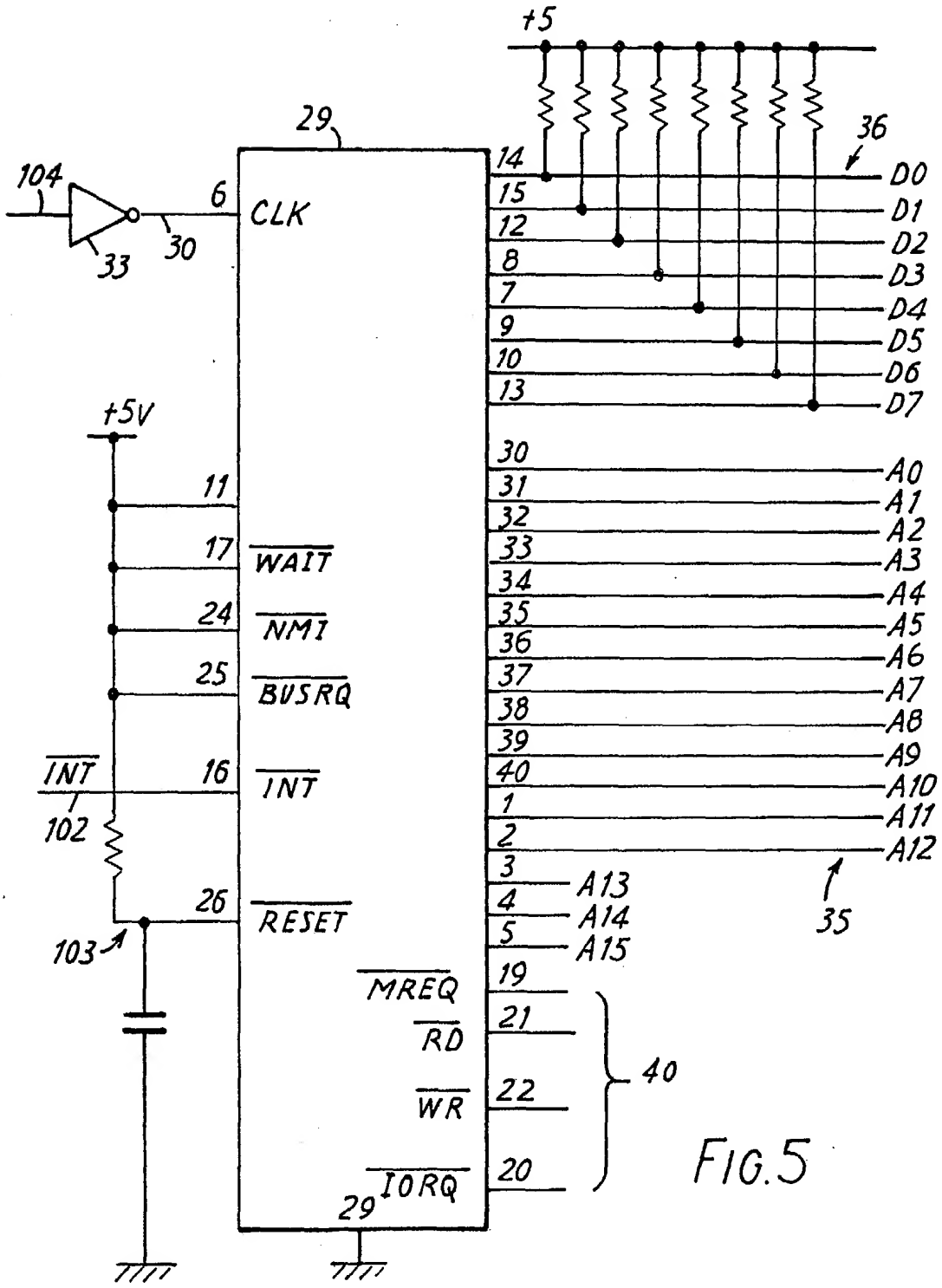
+5
29
36
104
6
CLK
33
30
14
15
12
8
7
9
10
13
D0
D1
D2
D3
D4
D5
D6
D7
+5V
11
17
WAIT
24
NMI
25
BUSRQ
INT
16
INT
102
26
RESET
103
30
31
32
33
34
35
36
37
38
39
40
1
2
3
4
5
A0
A1
A2
A3
A4
A5
A6
A7
A8
A9
A10
A11
A12
A13
A14
A15
35
MREQ
RD
WR
IORQ
19
21
22
20
40
29

FIG.5

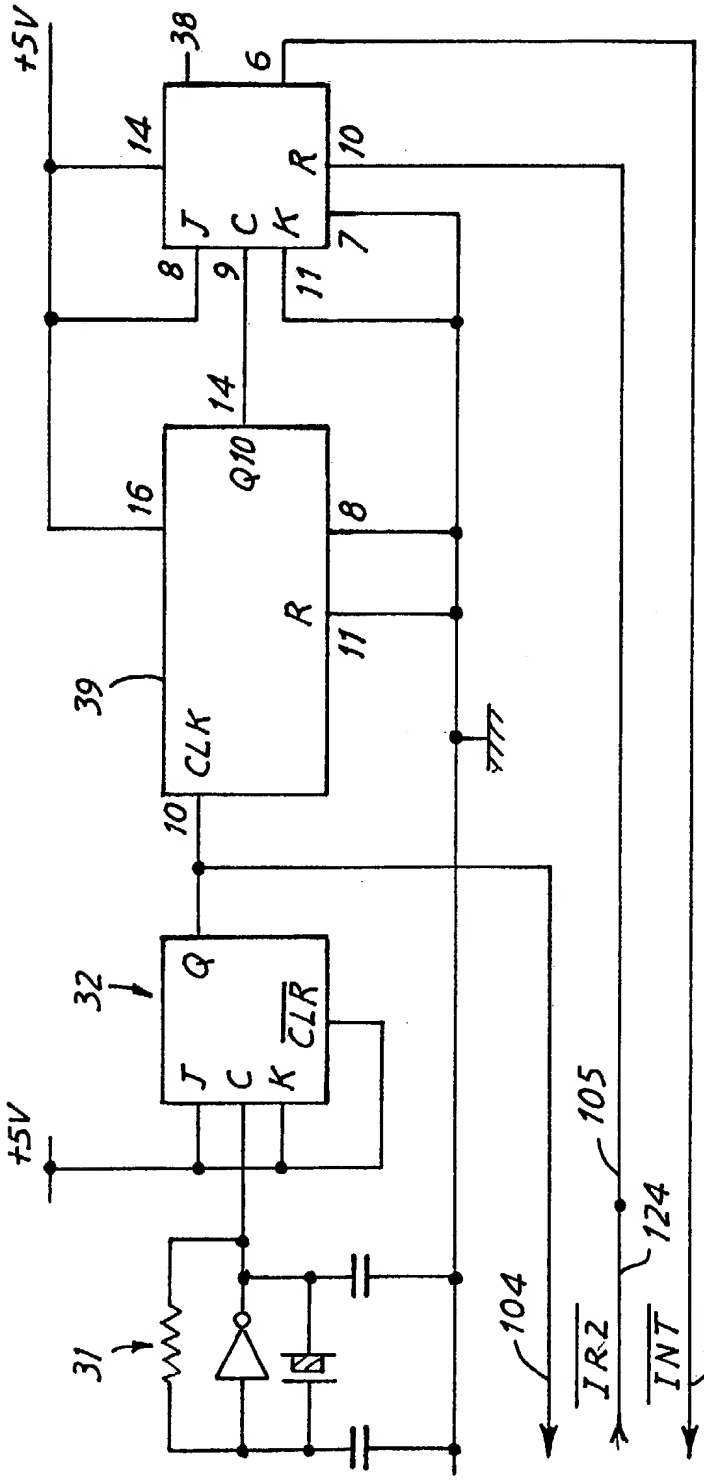
+5V
38
6
14
10
R
J
C
K
7
8
9
11
14
Q10
16
8
R
11
39
CLK
10
Q
32
CLR
J
C
K
+5V
105
124
31
104
IR2
INT
102

FIG.6

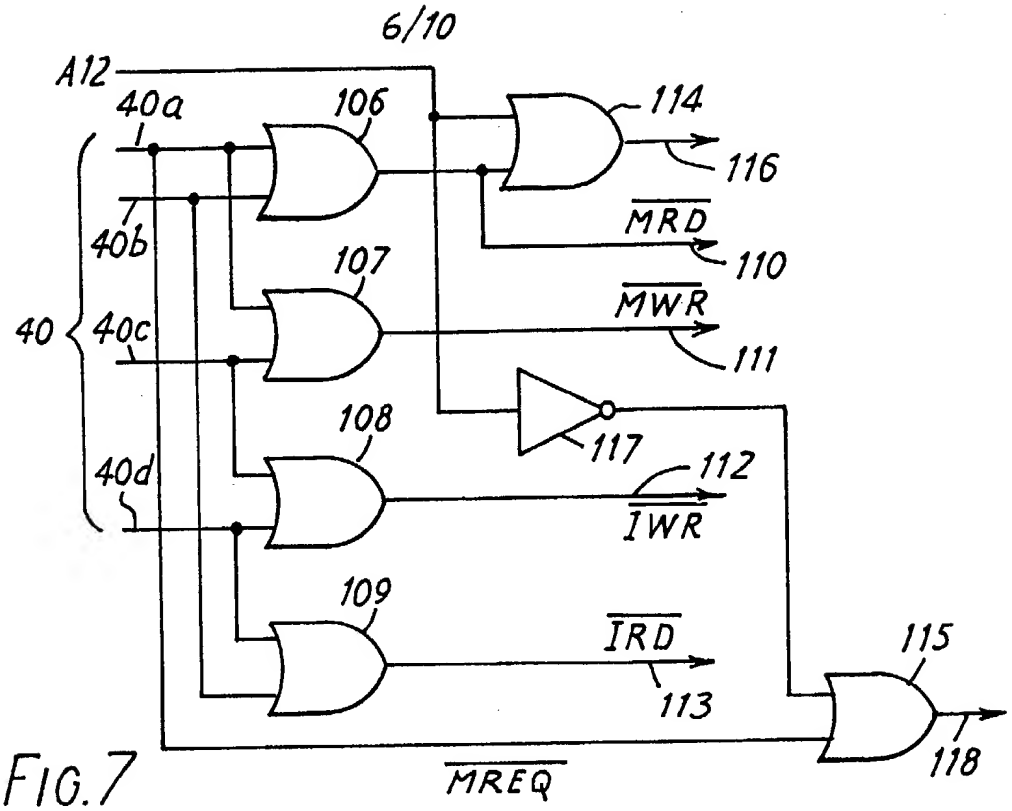
A12
40a
40b
40c
40d
40
106
107
108
109
114
116
MRD
110
MWR
111
117
112
IWR
IRD
113
115
118
MREQ

FIG. 7

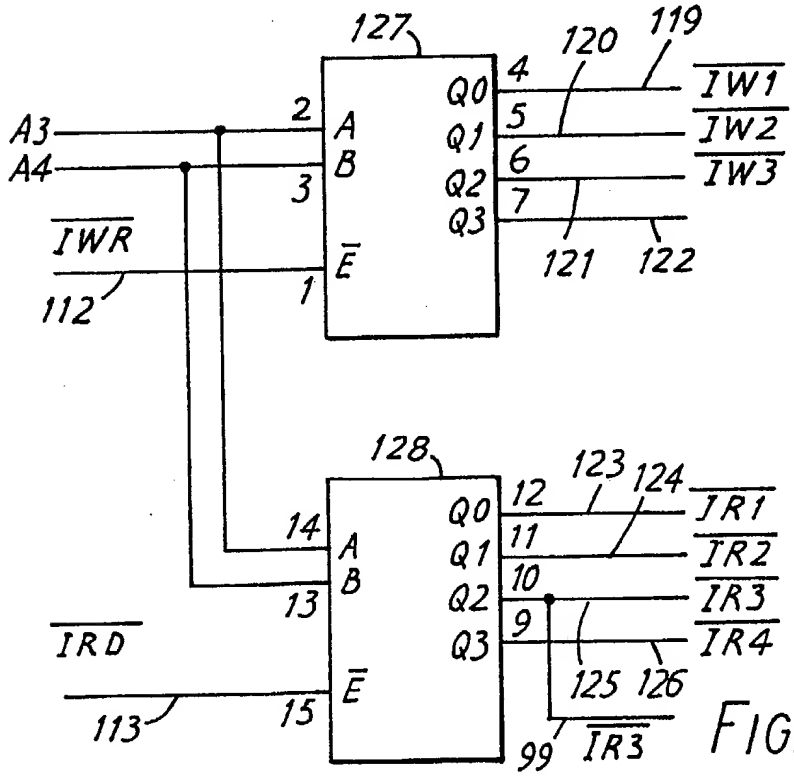
127
A3
A4
IWR
112
2
3
1
A
B
E
Q0
Q1
Q2
Q3
4
5
6
7
120
119
IW1
IW2
IW3
121
122
128
14
13
15
IRD
113
123
124
12
11
10
9
IR1
IR2
IR3
IR4
125
126
99
IR3

FIG. 8

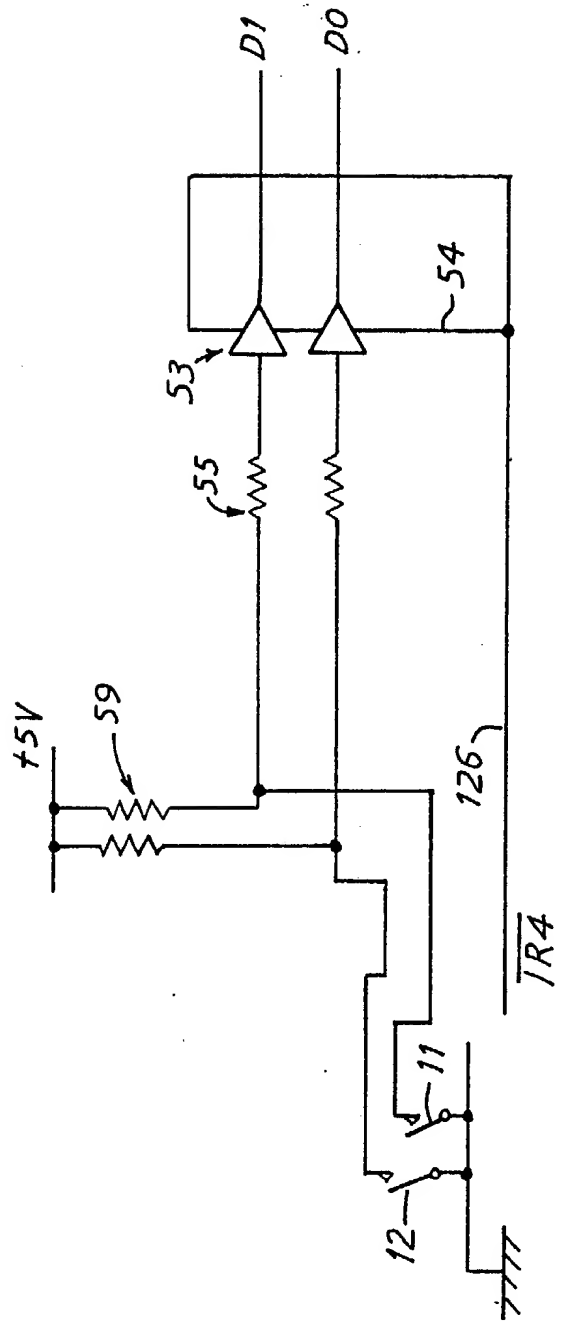

FIG. 9

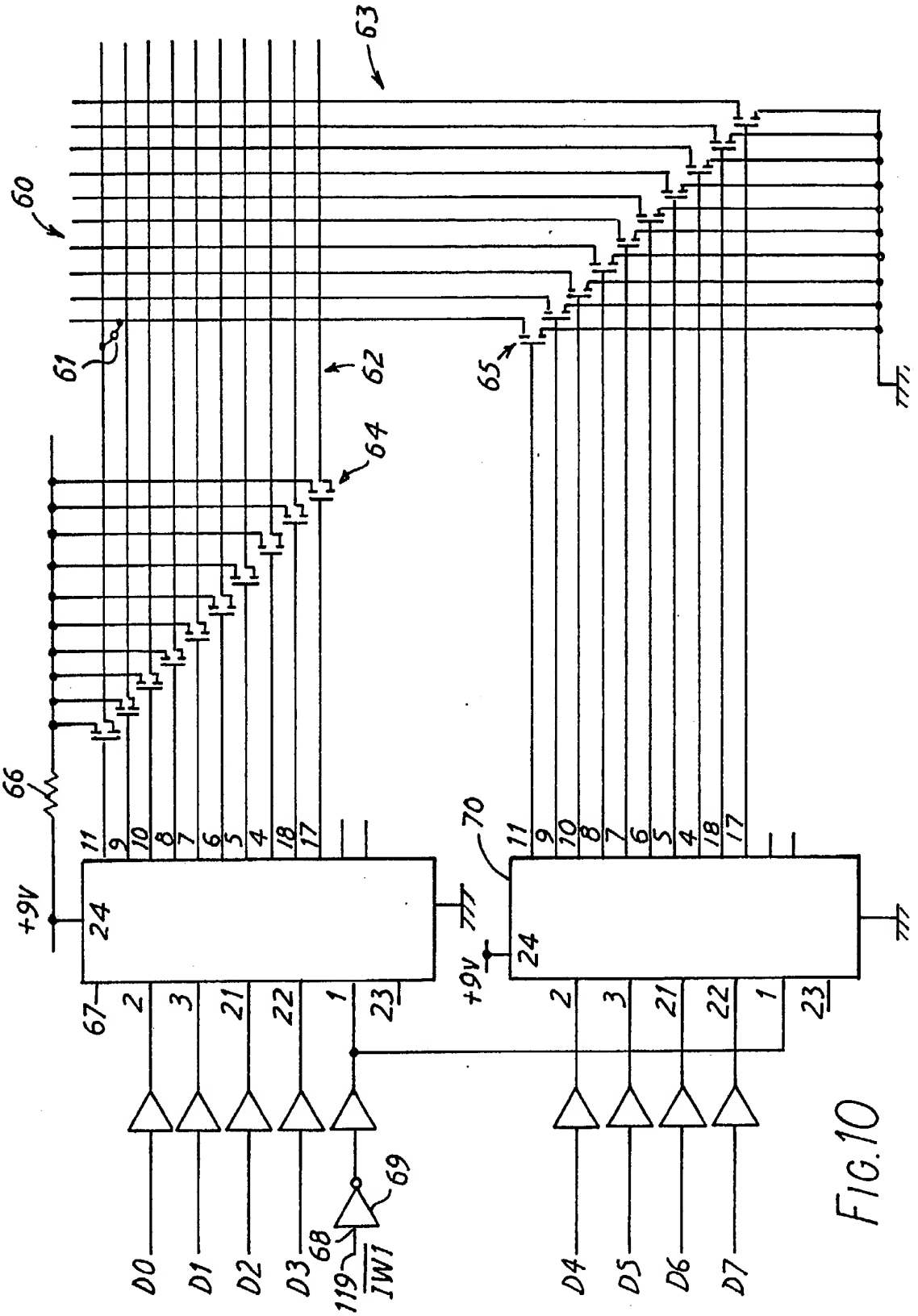
63
60
61
62
65
64
66
+9V
24
11
9
10
8
7
6
5
4
18
17
70
67
2
3
21
22
1
23
69
68
119
IW1
D0
D1
D2
D3
D4
D5
D6
D7

FIG.10

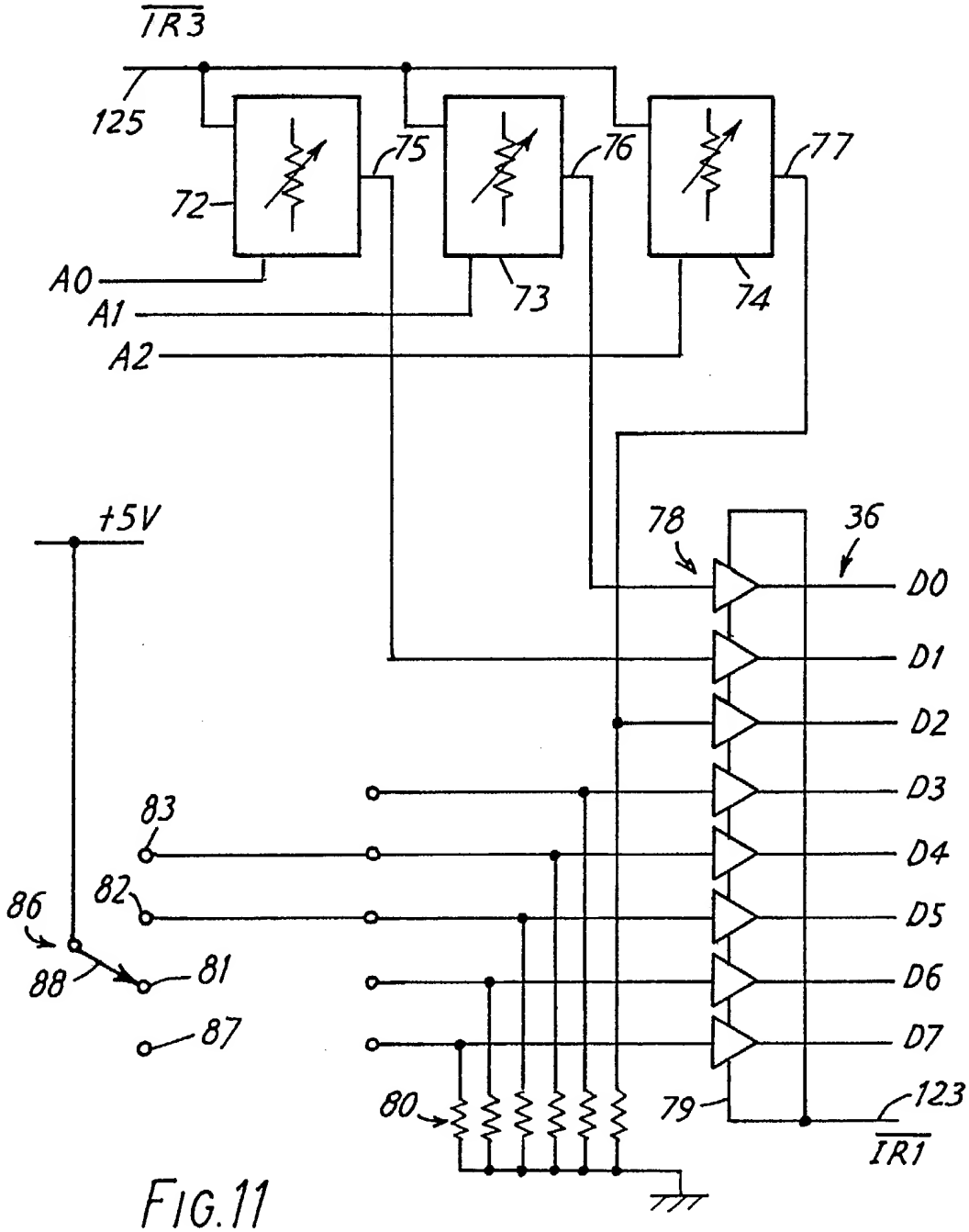
IR3
125
72
75
76
77
A0
A1
A2
73
74
+5V
78
36
D0
D1
D2
D3
D4
D5
D6
D7
83
82
86
88
81
87
80
79
123
IR1

FIG.11

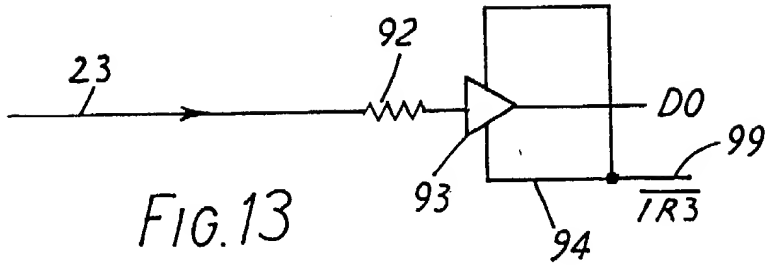
23
92
D0
99
93
94
IR3

FIG.13

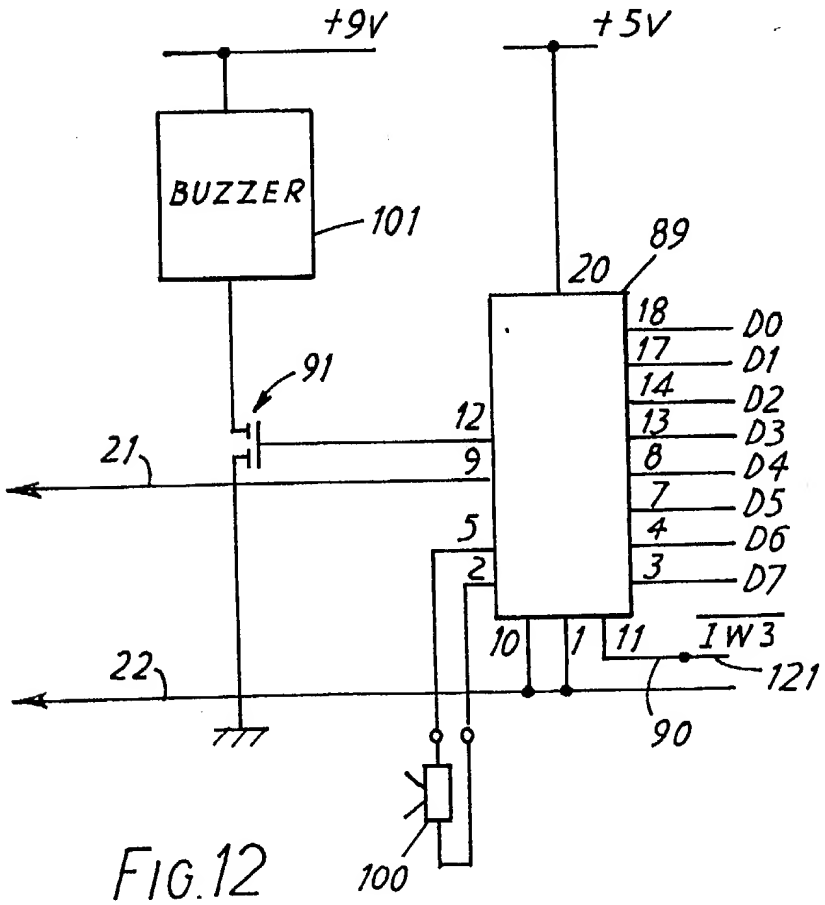
+9V
+5V
BUZZER
101
89
20
91
18
D0
17
D1
14
D2
13
D3
8
D4
7
D5
4
D6
3
D7
12
21
9
5
2
10
1
11
IW3
22
121
90
100

FIG.12

SPECIFICATION

Apparatus for controlling production of speech or text

This invention relates to apparatus for controlling production of speech or text.

In addition to ASCII code controlled printers there are now available speech synthesizers which are controllable by ASCII, for example the Votrax Type 'N talk speech synthesizer, available from Votrax, 500 Stephenson Highway, Troy, Michigan 48084, United States of America. As described in an article entitled "Add a Voice to your Computer" by Stan Miastkowski in Popular Computing, June 1982, at pages 81 to 86, the Votrax Type 'N Talk speech synthesizer converts ASCII code received through an RS232C connection into speech.

The present invention adapts a control apparatus for a display matrix, such as that described in U.K. patent application serial no. 2058419A, which can be used as a means of communication by a physically severely disabled person, to enable the apparatus to control a speech synthesizer or a printer, by providing a serial output of ASCII code signals. A particularly significant aspect of the adaption is that the storing of sequences of display matrix coordinates can be used as a means of composing complete sentences to be spoken by a speech synthesizer or printed out by a printer.

A preferred embodiment of the invention has a plurality of separately selectable message elements associated with each of the majority of the individually selectable regions of the display matrix, each such region being identificable by its respective matrix coordinates. For example, in a rectangular matrix display of rectangular panels, the panel in column 2 and row 2, numbered from the uppermost and the left-hand side respectively with the display treated as if in a vertical plane, may indicate four message elements such as the letter "a", "afternoon", "of" and "yes". Identification of the particular one of these four message elements can be effected by prior selection of an associated one of four panels respectively associated with one of four possible elements which may be indicated by each of the majority of the panels. Furthermore, by providing a means of distinguishing between different display overlays, for example by numbering the overlays and including in each an overlay selection panel to be activated followed by activation of the panel for indicating the number assigned to that overlay, a vocabulary limited only by memory capacity can be provided.

The invention will now be described in more detail, solely by way of example, with reference to the accompanying drawings, in which:-

Figure 1 is a schematic perspective view of control apparatus embodying the invention and coupled to a speech synthesizer unit, with, as an alternative, a printer;

Figure 2 is a block diagram illustrating connections between the control apparatus and the speech synthesizer unit of Figure 1,

Figure 3 is a simplified illustration of an overlay for a matrix display of the control apparatus of Figure 1,

Figure 4 is a block diagram of the control apparatus of Figures 1 and 2,

Figure 5 is a circuit diagram of a microprocessor unit of the control apparatus of Figure 4,

Figure 6 is a circuit diagram of timing circuitry included in the control apparatus of Figure 4,

Figure 7 is a circuit diagram of control logic in the apparatus of Figure 4,

Figure 8 is a circuit diagram of an input/output decoder of the apparatus of Figure 4,

Figure 9 is a circuit diagram of input circuitry of the apparatus of Figure 4,

Figure 10 is a circuit diagram of an LED matrix unit of the apparatus of Figure 4,

Figure 11 is a circuit diagram of a delays and scan mode selection unit of the apparatus of Figure 4,

Figure 12 is a circuit diagram of part of output circuitry and tone output control circuitry unit of the apparatus of Figure 4 and

Figure 13 is a circuit diagram of another part of the output circuitry and tone output control circuitry unit of the apparatus of Figure 4.

Figure 1 shows a display matrix control apparatus 10 embodying the invention and having an input switch device with two switches 11 and 12. Although two separate, manually operable switches 11 and 12 are shown, other input switch devices, having one or two switches and adapted to be operable by a physically severely disabled person, may be used. For example a two-switch breath-pressure activated unit or a pivoted plate switch unit may be used such as those supplied by Possum Controls Limited.

The display matrix control apparatus 10 is coupled through a lead 13 to a speech synthesizer unit 14 which in this example consists of a Votrax Type 'N Talk speech synthesizer combined with a suitable loudspeaker in a common housing. The unit 14 has a volumne control knob 15 and a frequency control knob 16 which controls the pitch of the synthesizer speech. As an alternative to the synthesizer unit 14, a printer 17, which is controllable by the same serial ASCII code signals as the synthesizer, can be coupled to the display matrix control apparatus 10 by a lead 18.

As indicated in Figure 2, the display matrix control apparatus 10 includes control and dictionary circuitry 20 and an indicator 19. The indicator 19 has rectangular array of one hundred LEDs (light emitting diodes) arranged in ten rows and ten columns to illuminate the one hundred panels of an overlay which may be as partially illustrated in Figure 3.

In use, one or both of the switches 11 and 12 are closed and opened to control the energisation of individual LEDs of the indicator 19. If the LED of the SPEAK panel of column 1 of the overlay shown in Figure 3 is selected, subsequent selection of indicator overlay panels containing message elements results in the synthesizer unit 14 producing the selected message element, selection of a message element including prior activation of one of the four panels inscribed A,B,C, and D of column 1, these being respectively associated with one message element in each panel. For example, if the B panel is selected before the panel in column 2, row 2, the

message element produced is "afternoon". To select a message element, the user must control the energisation of the LEDs of panels in a scanning mode starting from the HOME SQUARE panel. There are three scanning modes, modes 1, 2 and 3, which are as described in our co-pending patent application entitled Apparatus for entering characters into a data processing system, filed on 7th October 1982.

When a message element is selected, an observer can identify the intended element in any panel containing more than one element, by noting which one of the A,B,C and D panels is also illuminated. The control and dictionary circuitry uses the coordinates of these two panels as data for computing the address of the ASCII code corresponding to the selected message element, these codes being stored in tables held in a permanent memory region of the dictionary circuitry. The retrieved ASCII code is in parallel form and is outputted one bit at a time over a serial data transmission line 21 to the synthesizer unit 14, or to the printer 17 when this replaces the unit 14. A common ground line 22 is provided for the unit 14 and the circuitry 20. The synthesizer unit 14 also produces a busy signal on a line 23 when it is unable to accept data, and the busy signal line 23 is connected to the circuitry 20 to enable the circuitry 20 to delay transmission over the line 21 until the unit 14 is ready to receive.

The circuitry 20 includes a temporary store, divided into four regions, for messages. As in our corresponding application serial no. 2058419A, the user can store a message in a selected messae store by selecting the MEMORY WRITE LED followed by any one of the panels for the number 1,2,3 and 4. The stored message can be recalled for display by the indicator 19 by subsequent selections of the MEMORY READ LED followed by the appropriate number panel. Also, if SPEAK or PRINT is selected, the recalled display will be accompanied by the outputting of the ASCII codes over the line 21 corresponding to the recalled message elements. The temporary memory store stores only the matrix coordinates of the selected message elements, together with data identifying the level, i.e. which of the A,B, C and D panels the element is associated with, and the overlay number, which is a number identifying the particular overlay in use. For example, the overlay by Figure 3 may be designated overlay number 1.

The rate at which message elements are supplied to the unit 14 or the printer 17 can be varied by means of a manual control knob 24 provided on the unit 10 and controlling a variable resistor in the circuitry 20 which determines the time interval, hereinafter referred to as the recall delay, between message elements recalled for transmission and indication.

To facilitate the use of the unit 10 by a disabled user, the circuitry 20 requires a selection operation, i.e. selection of a panel of the overlay, at the input switch device by the user to be maintained for a suitable period of time before the selection is accepted. Thus accidental selections can be cancelled by abandonment of the selection operation before the expiry of a period referred to hereinafter as the actuate delay. The actuate delay is an adjustable time set by a variable resistor with a manually operable control knob 25 on the unit 10.

Where a two switch input device is used with the unit 10 as in Figure 1, the circuitry 20 operates the indicator 19 in one of the three scanning modes in which the LED of the home square is initially energised and any other panel is selected by the user controlling a scanning process in which the LEDs of successive panels are energised until the chosen panel is reached. In controlling these scanning processes, the user is required only to initiate and stop successive energisation, usually in columns and rows of panels. To enable such control, the energisation of each LED is maintained for a period of time referred to hereinafter as the scan delay. The scan delay is an adjustable time set by another variable resistor with a manually operable control knob 26 on the unit 10. To set the circuitry 20 in a condiction to carry out appropriate panel selection operations in response to different modes of user operation depending on user preference and/or the nature of the input switch device a mode selection switch with a manually operable control knob 27 is provided in the unit 10.

The unit 10 is shown in more detailed block diagram form in Figure 4.

The control and dictionary circuitry 20 includes a central processor unit 29 which receives a system clock signal at an input terminal 30 from a clock generator comprising a crystal oscillator 31 driving a divide-by-two circuit 32 coupled through an inverter 33. The processor unit 29 operates in accordance with a program stored in an erasable programmable read only memory (EPROM) 34 to which it is coupled by an address bus 35 and a data bus 36. Temporary storage is provided, as required by the program, by a random access memory (RAM) 37 connected to the two buses 35 and 36.

The program includes an interrupt routine which is run at regular internvals, each run of the interrupt routine being triggered by an interrupt signal supplied to the processor unit 29 by an interrupt generator 38 driven by the cyrstal oscillator 31 through the divide-by-two circuit 32 and a scaling counter 39. The rate at which the interrupt signal is generated determines the baud rate to the unit 14 or printer 17.

In operation, the processor unit 29 issues control signals over control lines 40 to a control logic unit 41 which gates these signals and an address line signal from the address bus 35 to produce further control signals to be applied to the EPROM 34, the RAM 37 and an input/output decoder 42 which also receives two address line signals from the address bus 35.

The input/output decoder 42 produces enabling signals for respective data input or output parts of a delays and scan mode selection circuitry 43, the indicator 19, user input circuitry 45 and output circuitry and audio tone control circuitry 46. An interrupt reset signal is also produced by the input/output decoder 42 at the beginning of each run of the interrupt routine and is supplied to the interrupt generator 38 to reset its output. The delays and scan mode selection circuitry 43 includes the variable resistors which can be adjusted by means of the

control knobs 24,25 and 26, and the mode selection switch with the control knob 27. The output and audio tone control circuitry 46 includes a buzzer and means for generating an audio tone at a frequency determined by the rate at which the interrupt routine occurs.

The input circuitry 45 includes the user's input switch device which is arranged to supply signals to one or two of the lines of the data bus 36 depending upon how many switches of the device are used.

Figure 5 shows the central processor unit 29, which is a Zilog Z80 microprocessor from Zilog (U.K.) Limited of Babbage House, Maidenhead, Berkshire SL6 1DU, and its connections to the output inverter 33 supplying system clock pulses, the interrupt generator 38 (at a line 102), the data bus 36, the address bus 35, and the four control lines 40 to the control logic 41. The conventional designations of Z80 control signals are shown in Figure 10 adjacent the input or output pins at which they occur in operation. It will be seen that the four control signals supplied to the control logic 41 are memory request $\overline{MREQ}$, read $\overline{RD}$, write $\overline{WR}$ and input/output request $\overline{IORQ}$. The pins for the wait signal $\overline{WAIT}$, non-maskable interrupt $\overline{NMI}$, and bus request $\overline{BUSRQ}$ are connected to the high signal level, 5 volts positive, permanently. A resistance-capacitance reset signal generator 103 is connected to the reset pin so that the processor 29 receives a reset signal $\overline{RESET}$ automatically on switching on the power supply to the system.

Figure 6 shows the circuitry of the crystal oscillator 31, divide-by-two circuit 32, counter 39 and interrupt generator 38. The crystal oscillator 31 hs component values such that the frequency of oscillation is, in the particular example, 2.4576 megahertz, so that system clock frequency is 1.2288 megahertz, the output of the divide-by-two circuit 32 being supplied on a line 104 to the inverter 33. The circuit 32 is a J-K flip-flop such as one unit of a dual J-K flip-flop type 74C107. The other unit of this dual J-K flip flop is shown as the interrupt generator 38. The Q output of the circuit 32 is supplied as the clock intput to a ripple counter, type 4040, serving as the counter 39. To obtain an output at 1200 hertz, the Q10 output of the counter 39 is taken and is supplied as the clock input to the interrupt generator 38. The reset signal produced by the input/output decoder 42 at the beginning of each interrupt routine is supplied as a signal $\overline{IR2}$ to the reset pin of the generator 38 over a line 105.

Figure 7 shows the control logic 41 which receives the control signals $\overline{MREQ}$, $\overline{RD}$, $\overline{WR}$, and $\overline{IORQ}$ from the processor 29 over the lines 40, and is also connected to address bus line A12. The individual lines 40 on which the signals $\overline{MREQ}$, $\overline{RD}$, $\overline{WR}$ and $\overline{IORQ}$ are transmitted are respectively referred to as lines 40*a*, 40*b*, 40*c* and 40*d*. The control logic 41 includes four OR-gates 106, 107, 108 and 109 so connected to the lines 40 that gate 106 receives the signals $\overline{MREQ}$ and $\overline{RD}$ as inputs, gate 107 receives the signals $\overline{MREQ}$ and $\overline{WR}$ as inputs, gate 108 receives the signals $\overline{IORQ}$ and $\overline{WR}$ as inputs, and gate 109 receives the signals $\overline{IORQ}$ and $\overline{RD}$ as inputs. The output signals from the gates 106 to 108 are respectively reffered to as the memory read sighals $\overline{MRD}$, the memory write signal $\overline{MWR}$, the input write signal $\overline{IWR}$ and the input read signal $\overline{IRD}$, which are produced on lines 100, 111, 112 and 113.

The logic 41 includes two further OR-gates 114 and 115. The OR-gate 114 receives the address signal bit on line A12 and the memory read signal MRD as inputs and provide output signals on a line 116. The OR-gate 115 receives the memory request signal $\overline{MREQ}$ from the line 40*a* and the inversion of the address signal bit on line A12 through an inverter 117, and provides output signals on a line 118.

Several EPROMS and RAM chips addressed by decoding address lines A10, A11 and A12 with a three to eight line decoder are used to implement the read only memory 34 and the random access memory 37.

The control logic 41 supplies the input write control signal $\overline{IWR}$ on line 112 and the input read control signal $\overline{IRD}$ on line 113 as input signals to the input/output decoder 42 which is shown in detail in Figure 8. The decoder 42 also receives the address bit signals on the A3 and A4 address lines, and produces on output lines 119 to 126 the control signals $\overline{IW1}$, $\overline{IW2}$, $\overline{IW3}$, $\overline{IR1}$, $\overline{IR2}$, $\overline{IR3}$ and $\overline{IR4}$.

The input/output decoder 42 is formed by a pair of two-to-four line decoders 127 and 128, which in this example are a dual two-to-four line decoder type 4556. Both decoders 127 and 128 receive the A3 and A4 address line signals at their input line pins. The line 112 supplies the input write control signal $\overline{IWR}$ to the enable pin of the decoder 127, and the line 113 supplies the input read control signal $\overline{IRD}$ to the enable pin of the decoder 128. The Q0, Q1 and Q2 output pins of the decoder 127 are connected respectively to the lines 119, 120 and 121, and the Q0 to Q4 output pins of the decoder 128 are connected respectively to the lines 123 to 126. The Q4 output pin of the decoder 127 is connected to the line 122 but no use made, in the present example, of the Q4 signals on this line. The lines 119, 121, 123 to 126, and 99 are connected as follows:-

line 119 to the input terminal 68 of the inverter 69 of the indicator circuitry shown in Figure 10;

line 121 to the clock input line 90 of the latch unit 89 in the output and audio tone control circuitry 46 shown in Figure 12;

line 123 to the enable signal line 79 of the tri-state buffers 78 of the delays and scan mode selection circuitry 43 shown in Figure 11;

line 124 to the reset signal line 105 of the interrupt generator 38 shown in Figure 6;

line 125 to the enable signal line 77 of monostable delay circuits of the delay circuitry shown in Figure 11;

30 line 126 to the enable signal line 54 of the tri-state buffers 53 of the input circuitry 45 shown in Figure 9; and line 99 to the enable signal line 94 of the tri-state buffer 93 of the circuit shown in Figure 13.

Thus the signals $\overline{IW1}$ and $\overline{IW3}$ are used as addressing or enabling signals to the data output ports of the indicator 19 and the output and audio tone control circuitry 46, and the signals $\overline{IR1}$, $\overline{IR2}$, $\overline{IR3}$ and $\overline{IR4}$ are used as addressing or enabling signals

to the data output port of the delays and scan mode selection circuitry 43, the interrupt generator 38, the delay monostables, the data input port of the input circuitry 45, and the data input port of the output control circuitry 46.

Figure 9 shows part of the input circuitry 45 connected to the two lines D0 and D1 of the data bus 36. The circuitry 45 includes an input port 53 formed by two tri-state buffers, each being a buffer of a hex tri-state buffer type 4503. The control terminals of these buffers are connected to a common control line 54 which receives a control signal $\overline{IR4}$ from the input/output decoder 42. In operation, both buffers 53 are either in their high impedance state or are presenting high or low signal levels to the respective lines D0 and D1. The input terminal of each buffer 53 is coupled through a respective resistor 55, of 100 kilohms in particular example, to respective terminals of the input switch 12 and the input switch 11. The input switches are connected through respective resistors 59 to a high signal level voltage rail, in this example at 5 volts positive. Thus if both input switches are open the input signal to each buffer 53 is a high signal which is applied to the respective data bus line when the control signal $\overline{IR4}$ goes low. To apply a low signal to any buffer 53, the respective input terminal of the D0 and D1 buffers must be connected to ground, which can be effected by closing the respective input switch 11 or 12.

Figure 10 shows circuitry for the indicator 19 which includes a LED matrix 60 in which, for simplicity, only one LED 61 is indicated. The matrix 60 has ten row conductors 62 and ten column conductors 63 providing one hundred connection points for LEDs. The LED at any particular point in the matrix 60 is energised whenever a respective one of ten row transistors 64 and a respective one of ten column transistors 65 are conductive, the row transistor 64 then providing a path from a positive voltage rail, of 9 volts in this example, through a resistor 66 to the anode of the LED, and the column transistor providing a path from the cathode of the LED to ground.

Each LED of the matrix 60 is arranged to act as the means of illuminating a respective one of the one hundred panels of the overlay of the indicator 19.

The row and column transistors 64 and 65 are field effect transistors operating as switches. The gate terminals of the row transistors 64 are connected to ten output pins respectively of a row decoder 67, which in this example is a four line to sixteen line decoder and latch, type 4514, having four input pins coupled by respective buffers to receive data from the D0 to D3 lines respectively of the data bus 36. A control signal $\overline{IW1}$ from the input/output decoder 42 can also be applied to the row decoder 67 on a line 68 coupled through an inverter 69 and another buffer to clock input pin of the row decoder 67. The D4 to D7 lines and the control line 68 are coupled in the same way to corresponding input pins of a column decoder 70, which also is a four line to sixteen line decoder and latch, type 4514, having ten output pins connected respectively to the gate terminals of the ten column transistors 65. It will be apparent that a LED matrix larger than the matrix 60 could be controlled by the decoders 67 and 70.

In operation, the row decoder 67, controlled by data on the D0 to D3 data bus lines, determines which row conductor 62 is active. The column decoder 70, controlled by data on the D4 to D7 data bus lines, determines which column conductor 63 is active. Thus the data lines D0 to D3 and the row decoder 67 can together be used to effect scanning in a "Y" direction in the matrix 60, and the data lines D4 to D7 and the column decoder 70 can together be used to effect scanning in an "X" direction in the matrix 60. Also, by alternate enabling of the decoders 67 and 70 and suitable data on the data bus 36, "diagonal" scanning can be effected by alternate steps in the X and Y directions.

Each of the decoders 67 and 70 has in the present example an input pin for a disable signal, pin 23 in the type 4514, to which a disable signal can be applied if developed elsewhere in the system to indicate a condition in which it is required that the matrix 60 should be completely extinguished.

To obtain sufficient brightness from the LEDs of the matrix 60, a substantially higher than normal current is passed through any LED which is to be energised. To avoid damage to the LEDs, the high current is passed intermittently only, the interrupt routine of the program being such that the row and column conductors 62 and 63 of any LED which is to be energised are rendered active only once in every eight runs of the interrupt routine, the interrupt routine being run 1200 times per second. The resistor 66 may be, for the 9 volt supply indicated, a 39 ohm resistor with a maximum rating of 4 watts. Hence by multiplexing, more than one LED can appear to be energised at the same time.

The circuitry 43 for delays and scan mode selection is shown in Figure 11. Three monostable delay circuits 72 73 and 74, each including a unit of a dual precision monostable integrated circuit type 4538 (not shown), are provided to set the scan delay, the actuate delay and the recall delay respectively. Each monostable delay circuit includes a variable resistor mechanically controlled by the respective knob 24, 25 or 26 of the unit 10. The variable resistor and a capacitor (not shown) together determine the time constant of the delay circuit and hence the value of the delay. The monostable delay circuits 72, 73 and 74 can be triggered when a control signal IR3 on a line 77 from the input/output decoder 42 is low, the scan delay monostable circuit 72 being triggered by a signal on the A0 address line of the address bus 35, the actuate delay monostable circuit 73 being triggered by a signal on the A1 address line of the address bus 35, and the recall delay monostable circuit 74 being triggered by a signal on the A2 address line. The output terminals 75, 76, and 77 of the monostable circuits 72, 73 and 74 are connected respectively to three of a set of eight tri-state buffers 78, type 4503, which are controlled by a control signal $\overline{IR1}$ on a line 79 from the input/output decoder 42. The output terminals of the tri-state buffers 78 are connected to respective data lines of the data bus 36 as shown in Figure 11, the output terminals of the circuits 72, 73 and 74 being thus coupled to the data lines D1, D0 and D2 respectively.

The input terminals of the six buffers 78 connected to the data lines D3 to D7 are coupled to ground through respective resistors 80 of, for example, 100 kilohms. The buffers for lines D4 and D5 are also connected to respective fixed contacts 83 and 82 of a mode selector switch 86 having two other fixed contacts 81 and 87 isolated, and a movable contact 88 mechanically controlled by the knob 27 of the unit 10. The movable contact 88 can be set in electrical contact with any one of the four fixed contacts 81 to 83 and 87, which are associated with input modes 1 to 3, and an OFF condition respectively. The input modes 1,3 and 3 are scanning modes in which user operation of an input switch device with the two switches 11 and 12 results in a scanning operation of the LED matrix 60. It will be seen from Figure 11 that mode 1 is a default mode, the fixed contact 81 being isolated. Thus even if the switch 86 is set in the OFF position, in which the movable contact 88 touches the fixed contact 87, mode 1 operation can be effected. It will also be seen that, for modes 2 and 3 a high signal level is applied from the movable contact 88 to the data lines D5 and D4 respectively.

In operation when the end of the scan delay, the actuate delay or the recall delay is being awaited, the buffers 78 are enabled sufficiently frequently by the control signal $\overline{IR1}$ for there to be only a negligible error in the sensing of the occurrence of the end of the delay. The range of scan delay values provided by the variable resistor of the scan delay circuit 72 is at least 0.2 secs to 2 seconds. The same minimum extent applies to the range of actuate delay values provided by its variable resistor.

Figure 12 shows part of the output circuitry and audio tone control circuitry 46. The circuitry 46 includes a latch unit 89, the example shown being an octal D flip-flop, type 74C374, having eight input pins connected respectively to the eight data bus lines D0 to D7. An enabling signal $\overline{IW3}$ from the input/output decoder 42 can be supplied to the latch unit 89 on a line 90 connected thereto. One of the output pins, at which signals on the data line D3 can be respectively latched, is connected to the gate terminals of a field effect transistor 91 arranged to act as a control switch for a buzzer 101 connected to a suitable supply (9 volts positive).

The two output pins of the latch unit 89 at which signals on the data lines D6 and D7 can be latched are connected respectively to the two input terminals of a ceramic sounder 100, for example type AT-27 of Projects Unlimited. In operation, an audio tone is produced from the sounder 100 by toggling the sounder inputs at the rate of occurrence of the interrupt routine, so that in the example of operation described hereinafter the sounder 100 can produce a tone at 1200 hertz.

The latch unit 89 is connected as shown to the common ground line 22 which is connected to the synthesizer unit 14 or the printer 17. Output pin 9 of the latch unit 89, at which the signals on the data line D4 can be latched, is connected to the data transmission line 21. In operation, ASCII codes are latched one bit at a time at the output pin 9 so that these codes are transmitted serially on the data transmission line 21.

Busy signals transmitted by the synthesizer unit 14 or the printer 17 are received by the circuitry 46 over the line 23 which, as shown in Figure 13, is coupled through a resistor, of 100 kilohms resistance for example, to a tri-state buffer 93 serving as an input port and connected to the data line D0 of the data bus 36. The control electrode of the buffer 93 is connected by a line 94 to the line 99 to receive the signal $\overline{IR3}$ from the input/output decoder 42.

The operation of the apparatus illustrated in Figure 4 will now be described in more detail.

The ROM 34 holds a program in which the Z80 processor unit 29 operates in its interrupt mode 1 in which in response to a low active interrupt signal $\overline{(INT)}$ the processor unit (CPU) 29 automatically branches to memory location 0038 (hexadecimal) after storing the return address of the main program in a stack region of the RAM 37. Operation of the Z80 microprocessor is described in Basic Principles and Practice of Microprocessors by D.E. Heffer, G.A. King and D.C. Keith, published by Edward Arnold (Publishers) Limited, 41 Bedford Square, London WC1B 3DQ in 1981, and other publications. Further details of the operation of the Z80 microprocessor can be obtained from Zilog (U.K.) Limited.

The interupt routine serves to output message data serially to the latch unit 89 of the output circuitry 46 and to control the energisation of the LEDs of the matrix 60, the latter function being effected substantially as in our copending application entitled "Apparatus for entering characters into a data processing system".

In outputting message data serially, the interrupt routine retrieves the value of a string length and the starting address of the temporary store, in the RAM 37, containing the ASCII codes to be transmitted, and, in successive runs of the interrupt routine, outputs successive bits of these ASCII codes until the string length has been counted down to zero. The interrupt routine includes a subroutine for transmitting a start bit and a subroutine for transmitting a stop bit. The particular bit to be transmitted is determined by the interrupt subroutine address stored in a temporary store, named RNEXT, whose contents are fetched at the beginning of each run of the interrupt routine. Each run ends with a subroutine which loads the address of the next such interrupt subroutine address into RNEXT. However, if the string length is zero, the interrupt routine is restricted to an initial subroutine which simply tests the string length value unless the busy signal is detected on data line D0 in which case this initial subroutine is restricted to the busy signal test alone. If the string length value is not zero, this value is decremented by one in the initial subroutine, the address of the beginning of the stored string to be transmitted is stored in a RAM store named RDATA, a RAM pointer, named RPOINT, which provided this last address is incremented by one, and the address of the interrupt subroutine for outputting the first bit of the string is loaded into RNEXT.

Each subroutine for outputting a bit to the latch unit 89 for transmission over the line 21 puts either 1 or 0 on the data line D4. This is done by testing the respective bit in the string, and if it is 1, transmitting

0 over the data line D4, and if the respective bit is 0, transmitting 1 over the data line D4, to the latch unit 89. The inversion is necessary to ensure that RS232 compatible voltages are presented on the transmission line 21.

The interrupt routine of the program in the ROM 37 then has a stem section in which a value stored in a temporary storage region, referred to hereinafter as TIMER1, is decremented, the condition (status) of the inputs of the ceramic sounder 100 is toggled, and one of eight different subroutines, referred to hereinfter as MOD0, MOD1, MOD2, MOD3, MOD4, MOD5, MOD6 and MOD7 is carried out before the return to the main program. The value in TIMER1 is started from a number referred to hereinfter as TIME1 which when counted down at the 1200 hertz rate of the interrupt routine provides a time suitable for the duration of an audio tone output from the ceramic sounder 100. When the value in TIMER1 is zero, the interrupt routine jumps round the toggling of the inputs to the sounder 100, so that the sounder 100 is silent when TIMER1 contains zero.

The eight subroutines MOD0 to MOD7 control the operation of the LED matrix 60 of the display 19. To ensure that excessive power is not supplied to any LED, data commanding the illumination of LEDs in accordance with the user's input to the input circuitry 45 is not used directly to control the LEDs but is stored in seven temporary storage regions of the RAM 37 designated SLOT0 SLOT1, SLOT2, SLOT3, SLOT4, SLOT5 and SLOT6, and is transferred, in a multiplexing operation effected by the interrupt routine in such a way as to ensure that no LED can be energised more than once in every eight passes of the interrupt routine, to seven further temporary storage regions of the RAM 37 designated MUX0, MUX1, MUX2, MUX3, MUX4, MUX5 and MUX6. The data stored in any of the regions SLOT0 to SLOT6 and MUX0 to MUX6 is the matrix coordinates of an LED of the matrix 60 or a blank code (FF hexadecimal). The presence of LED coordinates in any of MUX0 to MUX6 results in energisation of the LED having those coordinates. The presence of the blank code FF in any of MUX0 to MUX6 results in no LED of the matrix 60 being energised during a subroutine in which the contents of the MUX region containing the blank code are outputted. The seven subroutines MOD0 to MOD6 output the contents of the regions MUX0 to MUX6 respectively. The subroutines MOD2, MOD3, MOD5 and MOD6 are concerned only with the outputting of the respective MUX contents.

MOD0 and MOD4 output the contents of MUX0 and MUX4 respectively and also carry out the obtaining of input data from the input circuitry 45, including the debouncing of this data. The form of debounced data produced, is appropriate for inputs from input switch devices in which only one switch can be operated at any time, such as the device having the two switches 11 and 12 mechanically shielded against concurrent operation. Four temporary storage regions of the RAM 37 are used, designated INSTAT, IPSTAT, DESTAT and DESTAT+1, in this process. The region IPSTAT is used as a debounce timer, being loaded at appropriate instants with a value, in this example OA (hexadecimal), which is decremented to give the debounce time. The data stored in INSTAT is the data from the buffers 53 of Figure 9 present when the debounce timer last stopped running or present immediately after the first change in the data which occurred from the condition existing before the debounce timer started running from a non-running condition. The debounce timer starts running each time there is a change in the data from the buffers 53, so that if a change occurs while the debounce timer is running, the timer is re-started, i.e. the timer starts running from a running condition. Consequently a sequence of changes in the data from the buffers 53 which occur sufficiently close together for the debounce timer to run continuously from the occurrence of the first change until the end of the debounce time after the last change causes the data in INSTAT to register only the data appearing after the first and last changes in the sequence. The data stored in DESTAT is debounced in a conventional manner, the current input data from the buffer 53 only being stored in DESTAT when the debounce timer, IPSTAT, reaches zero. The region DESTAT+1 is used to temporarily store current input data for comparison purposes a change store current input data for comparison purposes a change in the data from the buffers 53 being detected by comparing the current input data received from the buffers 53 with the data stored in DESTAT+1 at the previous run of a subroutine in which the debounce process is carried out, i.e. in MOD0 or MOD4. In the debounce process, in MOD0, or MOD4, carries out the following steps:

1) The outputs of the buffers 53 are read (new input data).

2) The new input data is compared with the contents of DESTAT+1 (previous input data).

3) If the new and previous data are the same, the debounce timer is tested for expiry (contents of IPSTAT compared with zero).

4) If the debounce timer has expired, the new input data is stored in INSTAT and DESTAT.

5) If the debounce timer has not expired, the contents of IPSTAT are decremented.

6) If at the comparison in step 3 the new and previous data are different, the debounce timer is tested for expiry.

7) If the debounce timer has expired, the debounce timer is restarted (OA hexadecimal loaded into IPSTAT), then decremented.

8) The new input data is stored in INSTAT.

9) If in step 7 the debounce timer has not expired, the debounce timer is restarted, and then decremented. No further debounce action is then taken in this run of MOD0 or MOD4.

It will be seen that in this way, INSTAT is up-dated by a change in input occuring when the debounce timer is not running, and when there has been sufficient time since the last change while the timer is running for the timer to expire, and DESTAT is only up-dated in the latter circumstances.

Since MOD0 and MOD4 both contain the debounce process, the outputs of the buffers 53 are read 600 times per second. Changes which occur and disappear between two successive readings of the buffers 53 have no effect.

The subroutine MOD7 carries out two processes: a process which results in the LED whose coordinates are stored in SLOT0 being flashed while a flash timer, which is a temporary store region designated TIMERL in the RAM 37, is running; and a process in which the contents of SLOTs 1 to 6 are transferred to MUX1 to 5 and MUX0 respectively in accordance with priority rules which cause the blank code FF (hexadecimal) to be loaded into any one or more of MUX 1 to 5 and MUX0 If the coordinates stored in the corresponding SLOT are the same as those stored in a SLOT of higher priority. THe order of priorty is SLOT0, SLOT1, SLOT2, SLOT3, SLOT4, SLOT5, SLOT6. In carrying out the flash process, MOD7 includes the step of decrementing the value in TIMERL, and testing for zero. If the value after decrementing would be zero, the blank code is loaded into SLOT0. When the flash timer is running, bit 5 of TIMERL is tested and either the contents of SLOT0 or the blank code FF is loaded into MUX6 depending on the state of this bit 5. Bit 5 is used since it changes at a suitable rate for a flashing effect when SLOT0 contains the coordinates of a LED.

In the main routine of the program, SLOT6 is used to store the coordinates of the LED to be energised in any scanning processes. SLOT0 is used to store the coordinates of the LED of the panel selected by the user Thus when the user is searching for the desired panel, LEDs will be illuminated steadily in accordance with transfer from SLOT6 to MUX0. When the user selects a panel, its LED will flash for a time determined by the value in TIMERL.

Since SLOT1 to SLOT6 can store and transfer to MUX 1 to 5 and MUX0 up to six different LED coordinates, up to six different LEDs can be effectively illuminated together. The main routine stores the coordinates for selections such as SHIFT, A,B,C,D, OVERLAY, SELECT, MEMORY, WRITE, MEMORY READ, in SLOT1 to SLOT5.

The eight MOD subroutines are included respectively in eight successive runs of the interrupt routine by the use of the index register X of the Z80 processor 29, the sequence being MOD7 followed by MOX0 to MOX6. Each MOD routine loads the index register X with the address for the next MOD routine.

The main program routine starts by establishing interrupt mode 1 and jumping past the interrupt routine to an initialization process in which the stack pointer register of the CPU 29 is initialized, a number of temporary storage regions in the RAM 37 are put into initial conditions, the address for MOD7 is loaded into index register X. In this process, SLOT6 is loaded with the coordinates of the HOME SQUARE LED, and the blank code FF is loaded into SLOT0 and SLOT2 to SLOT5. The value 01 hexadecimal is loaded into SLOT1 to establish energisation of the A panel LED. Also, a starting value, designated TIMEL, is loaded into TIMERL, and a suitable value is loaded into each of INSTAT, IPSTAT, DESTAT and DESTAT+1. Also the starting address of a subroutine in the interrupt routine which implements transmission of a stop bit on the line 21 is loaded into RNEXT.

The initialization process ends by enabling interrupts and jumping to a monitoring subroutine labelled MONIT1.

In the monitoring subroutine, the scan mode selector switch 86 is read through the buffers 78 and one of three input mode subroutines labelled MODE1 to MODE3 is jumped to depending on the setting of the switch 86. The chosen 20 input mode subroutine controls the LED matrix 60. Each input mode subroutine ends either with a return to HOME SQUARE or selection of a special function or a message element to be implemented or entered into the memory 37. After selection has occurred, the detection of any special function is carried out and if the selection is not a special function, the selected message element is communicated or stored.

When a message element is to be sent to the unit 14 or printer 17 the coordinates of the LED for that character on the indicator 19 are used to locate the ASCII code in a look-up table stored in the ROM 34. Two such look-up tables are stored in the ROM 34, one for the speech mode and the other for the printing mode.

The main routine of the program also includes several processes for indicating, by the use of the sounder 100 and flashing of LEDs, that various user operations are errors. In general, whenever the sounder 100 is required to start producing a tone, the value TIME1 is loaded into TIMER1. Similarly, whenever a LED is requested to start flashing, the starting value TIMEL is loaded into TIMERL, and the coordinates of the LED must either already be in SLOT0 or be loaded in to start the flashing. The duration of a tone can be prolonged by restarting TIMER1 by loading TIME1 in again before the value in TIMER1 reaches zero. To avoid interference with the bit in TIMERL which determines the state of the flashing LED, restarting of TIMERL, when required, is effected by carrying out a logic OR operation on the contents of TIMERL with the value CO hexadecimal, thereby setting only the two most significant bits in TIMERL. In a particular example, the value of TIMEL is chosen to give three flashes over substantially 4 seconds. The time TIME1 may be 50 hexadecimal. The value OA hexadecimal in IPSTAT gives a debounce time of 1/30 seconds with an interrupt rate of 1200 hertz.

The monitoring subroutine MONIT1 and the three input modes MODE1, MODE2 and MODE3 are as described in our copending patent application entitled "Apparatus for entering characters into a data processing system". When the chosen input mode indicates that a selection has been made by the user, the coordinates of the selected LED are tested to establish whether a special function or a message element has been selected. The test successively eliminate CALL, SHIFT, OVERLAY SELECT, A or B or C or D, TONE ON/OFF, and any further special functions included such as FEED. Each test is performed by comparing the matrix coordinates, i.e. the column and row numbers, which identify the LED of the selected indicator panel, with the matrix coordinates of the special function being tested for. If all these tests are negative, the selected LED must be that of a message element panel or MEMORY WRITE, MEMORY READ, SPEAK or PRINT. Accordingly the selected LED coordinates are compard with those of MEMORY WRITE. If this test is negative, a

temporary storage (RAM) region named MEMORY is tested to discover whether MEMORY WRITE has already been selected in a previous selection operation. If this test is negative, the selected LED coordinates are compared with those of MEMORY READ. If this test is negative, MEMORY is tested to discover whether MEMORY READ has already been selected in a previous selection operation. If this test is negative, selection of SPEAK is tested, then selection of PRINT, and finally a temporary store named TABFLG is tested to discover whether the selection is to be indicated only by the indicator 19 or is to be transmitted over the line 21. There is then either immediate return or return after setting up data to be transmitted, as a result of the operation of the interrupt routine, to flashing of the selected LED and updating of temporary stores for overlay selection and shift status before the HOME SQUARE coordinates are loaded into SLOT6.

To set up data to be transmitted, the starting address in the appropriate look-up table, which depends on whether the output is for speech or printing (text), the particular overlay in use on the indicator 19 (overlay number), and the message element "level" in operation (i.e. A,B,C or D), is computed first from the stored status data relating to these factors. The coordinates of the selected LED are effectively a decimal number identifying the LED in the series 1 to 100 formed by the coordinates of all the LEDs. The selected LED coordinates are therefore converted into the corresponding hexadecimal number and the relative address of the beginning of the string to be transmitted computed by incrementing the look-up table address, derived from the factors mentioned above, by the hexadecimal number obtained from the selected LED coordinates. The contents of the final look-up table address thus computed are stored in a temporary storage region (RAM) named RBUFF unless the contents are an end of string code, the starting address of RBUFF being stored RPOINT. The process of storing a string in RBUFF is carried out one byte (i.e. eight bits) at a time, the number of bytes stored being itself stored in RSTAT unless zero. The number bytes in the string length which is decremented by one at reach run of the interrupt routine. The main routine waits for RSTAT to be decremented to zero after being loaded with the string length. When the string length has thus been counted down, and therefore the string transmitted, either on ASCII SPACE code, or on ASCII CARRIAGE RETURN code and an ASCII LINE FEED code is stored in a location pointed to by RPOINT.

Further subroutines are provided for adding shift data to the codes to be transmitted where required.

When MEMORY WRITE is first selected, 04 hexadecimal is stored in MEMORY. It is then necessary to select one of the panels for indicating the numerals 1,2,3 and 4. The main routine tests for such a valid selection and if one is found, the corresponding hexadecimal code 00,01,02 or 03 is respectively stored in MEMORY. From this memory code and the starting address of a temporary storage region named BUFF a memory buffer stored is defined and an end of message deliniting code, overlay, level and shift data stored there. The address of the next available location in the memory buffer store is then stored in a RAM pointer and the number of bytes already stored in this store is also stored. A subsequent selection of an LED results in a series of tests to eliminate illegal selections such as MEMORY READ, SPEAK and PRINT, and in processing of a valid selection, i.e. DELETE or a message element. Selection of DELETE results in emptying of the memory buffer store. Selection of a message element results in the coordinates of the selected LED being stored in the next available location of the memory buffer store, the associated pointer and byte counter being incremented accordingly. Message elements can thus be stored in one of the four memory buffer store regions until that region is full. The memory buffer store byte counter is tested for overflow at each storing of a message element. If overflow is found, an error subroutine is carried out which results in the indicator 19 flashing the HOME SQUARE LED.

To obtain recall of a message stored in the memory buffer store, MEMORY READ is selected, and then the panel of the number 1,2,3 or 4 of the store into which the message was written must be selected. If this is done correctly, the selection of the correct number panel leads to the computing of the required starting address in the memory buffer store from the starting address of BUFF and the code stored in MEMORY. The first data retrieved is the overlay number, the level and shift status. The stored selections are then retrieved and tested to determine whether they represent message elements to be transmitted or special functions to be executed. If they represent message elements, the stored coordinates are treated as described hereinbefore to produce from the appropriate look-up table ASCII codes to be transmitted. If they represent special functions, there is no transmission.

The operation of the sounder 100 can be inhibited by selection of the TONE ON/OFF LED, successive selections of this LED in effect toggling operation of the sounder 100.

CLAIMS

1. Apparatus for controlling production of speech or text, the apparatus including user operable input switch means coupled to selector means for determining a message element to be produced as an element of speech or text, the selector means operating in response to operation of the input switch means in accordance with a predetermined mode of operation, a memory storing speech and text element codes corresponding to message elements which can be determined and indicated by the selector means, and means for retrieving a corresponding code from the memory in response to operation of the selector means to determine a message element and present the said corresponding code as an output signal.

2. Apparatus according to claim 1, wherein the said retrieving and presenting means is such as to present the said corresponding code as a serial output signal.

3. Apparatus according to claim 1 or 2, wherein the said corresponding codes are ASCII codes.

4. Apparatus according to any preceding claim, wherein the selector means includes an indicator for indicating visibly message elements determined by operation thereof.

5. Apparatus according to any preceding claim wherein the retrieving and presenting means includes a processor and temporary memory coupled thereto.

6. Apparatus according to claim 1 and substantially as described hereinbefore with reference to the accompanying drawings.

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